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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PATEL, NIKETA I

ART UNIT	PAPER NUMBER
2182	4

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>12 March 2003</u> .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-13 and 15-20</u> is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-13, 15-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

     If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____ .

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

     a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)   4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5)☐ Notice of Informal Patent Application (PTO-152)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   Claims 1-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Nguyen et al. U.S. Patent Number: 5,887,163 (hereinafter referred to as "*Nguyen*") and further in

view of Poisner U.S. Patent Number: 6,421,765 (hereinafter referred to as "*Poisner*".)

3.   Referring to claim 1, *Nguyen* teaches a data processing system operable with at least two

types of software (see *Nguyen* column 3 – lines 56-65; column 4 – lines 13-46), the system

comprising: a host interface (see *Nguyen* column 8 – lines 9-58; figure 7 – element 724, 716,

710, 718, 720, 722) for providing address, data and control signals from a host (see *Nguyen*

column 8 – lines 9-67; column 4 – lines 13-46), a storage element for holding data accessible via

the host interface (see *Nguyen* column 8 – lines 9-67; column 4 – lines 13-46; figure 7 – element

710), and accessing the storage element so as to access the data as a first data element in a first

register when the system operates with a first type of software, and as a second data element in a

second register when the system operates with a second type of software (see *Nguyen* column 3 –

lines 56-65; column 4 – lines 13-46). *Nguyen* fails to explicitly set forth the limitation of an

alternate access circuitry for providing access to the storage element. However, *Poisner* discloses

an access circuitry for providing access to the different registers in the storage element based on

the received signal (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-2; column 1 – lines 39-47; figure 1 – element 14c, 14a and 14b, 14, 16, 12), reducing extra signals or signal lines that are used to access the memory elements.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the system of *Nguyen* to be implemented with an access circuitry to provide access to first register and a second register to reduce the extra signals or signal limes that are normally used to access the registers. It is for this reason that one of ordinary skill in the art would have been motivated to substitute *Nguyen's* system with an access circuitry to improve versatility of a computer system by reducing the extra signals or signal lines that are used to access the registers.

4.   Referring to claim 2, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches an alternate access circuitry is configured to perform writing data into the storage element in response to a fist address signal supplied from the host interface to access the first register, when the system operates with the first type of software (see *Poisner* column 2 – lines 57-67; column 3 – lines 1-14.)

5.   Referring to claim 3, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches an alternate access circuitry is configured to perform writing data into the storage element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software (see *Poisner* column 2 – lines 29-67; column 3 – lines 1-14.)

6.   Referring to claim 4, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches an alternate access circuitry is configured to perform reading

data from the storage element in response to a first address signal supplied from the host

interface to access the first register, when the system operates with the first type of software (see

Poisner column 2 – lines 29-67; column 3 – lines 1-14.)

7.   Referring to claim 5, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 1 above, teaches an alternate access circuitry is configured to perform reading

data from the storage element in response to a second address signal supplied from the host

interface to access the second register, when the system operates with the second type of

software (see *Poisner* column 2 – lines 29-67; column 3 – lines 1-14.)

8.   Referring to claim 6, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 1 above, teaches an alternate access circuitry (see *Poisner* figure 1 – element

14c) comprises a writing multiplexer (see *Poisner* figure – element 14c; column 1 – lines 39-

47) having a first input for supplying the first data element to the storage element when the

system operates with the first type of software, and a second input for supplying the second data

element to the storage element when the system operates with the second type of software (see

Poisner column 2 – lines 5-67; column 3 – lines 1-14.)

9.   Referring to claim 7, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 1 above, teaches a writing multiplexer is controlled by a first select signal to

pass the first data element to the storage element when the first select signal is asserted (see

Poisner column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-47.)

10.   Referring to claim 8, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 1 above, teaches a writing multiplexer is controlled by a second select signal to

pass the second data element to the storage element when the second select signal is asserted (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-47.)

11.   Referring to claim 9, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches a first select signal is asserted in response to a fist address signal supplied from the host interface to access the first register (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-47.)

12.   Referring to claim 10, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches a second select signal is asserted in response to a second address signal supplied from the host interface to access the second register (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-47.)

13.   Referring to claim 11, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches an alternate access circuitry (see *Poisner* figure 1 – element 14c) comprises a first reading gate (see *Poisner* figure – element 14c; column 1 – lines 39-47) coupled to the storage element for outputting the first data element when the system operates with the first type of software, and a second reading gate coupled to the storage element for outputting the second data element when the system operates with the second type of software (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-47.)

14.   Referring to claim 12, the system of *Nguyen* as modified by the teachings of *Poisner* as applied to claim 1 above, teaches a first reading gate is configured to output the first data element in response to a first address signal supplied from the host interface to access the first register (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-47.)

15.   Referring to claim 13, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 1 above, teaches a second reading gate is configured to output the second data

element in response to a second address signal supplied from the host interface to access the

second register (see *Poisner* column 2 – lines 5-67; column 3 – lines 1-14; column 1 – lines 39-

47.)

16.   Referring to claim 15, *Nguyen* teaches a network interface comprising: a host interface

(see *Nguyen* column 8 – lines 9-58; figure 7 – element 724, 716, 710, 718, 720, 722) for

supplying address, data and control signals from a host (see *Nguyen* column 8 – lines 9-67;

column 4 – lines 13-46), a storage element for holding a data element accessible via the host

interface (see *Nguyen* column 8 – lines 9-67; column 4 – lines 13-46; figure 7 – element 710),

and providing multiple paths for accessing the data element, and configured to select a path for

accessing the data element depending on a type of software used to operate the network interface

(see *Nguyen* column 3 – lines 56-65; column 4 – lines 13-46.) *Nguyen* fails to explicitly set forth

the limitation of an alternate access circuitry for providing access to the storage element.

However, *Poisner* discloses an access circuitry for providing access to the different registers in

the storage element based on the received signal (see *Poisner* column 2 – lines 5-67; column 3 –

lines 1-2; column 1 – lines 39-47; figure 1 – element 14c, 14a and 14b, 14, 16, 12), reducing

extra signals or signal lines that are used to access the memory elements.

One of ordinary skill in the art at the time of applicant's invention would have clearly

recognized that it is quite advantageous for the system of *Nguyen* to be implemented with an

access circuitry to provide access to first register and a second register to reduce the extra signals

or signal limes that are normally used to access the registers. It is for this reason that one of

ordinary skill in the art would have been motivated to substitute *Nguyen's* system with an access

circuitry to improve versatility of a computer system by reducing the extra signals or signal lines

that are used to access the registers.

17.   Referring to claim 16, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 15 above, teaches a path for accessing the data element is allocated in response

to an address signal supplied from the network interface to access a predetermined register, when

a selected type of software is used to operate the network interface (see *Poisner* column 2 – lines

29-67; column 3 – lines 1-14.)

18.   Referring to claim 17, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 15 above, teaches that a selected type of software requires the data element to be

held in the predetermined register (see *Nguyen* column 3 – lines 56-65; column 4 – lines 13-46.)

19.   Referring to claim 18, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 15 above, teaches a method of providing access to a storage element for holding

a data element, comprising the steps of: accessing the storage element via a first access path

when a first type of software is used to operate the data processing system, and accessing the

storage element via a second access path when a second type of software is used to operate the

data processing system (see *Poisner* column 2 – lines 29-67; column 3 – lines 1-14.)

20.   Referring to claim 19, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 15 above, teaches the first access path is allocated in response to a first address

signal identifying a first register required by the first type of software to hold the data element

(see *Poisner* column 2 – lines 29-67; column 3 – lines 1-14.)

21.   Referring to claim 20, the system of *Nguyen* as modified by the teachings of *Poisner* as

applied to claim 15 above, teaches the second access path is allocated in response to a second

address signal identifying a second register required by the second type of software to hold the

data element (see *Poisner* column 2 – lines 29-67; column 3 – lines 1-14.)

Response to Arguments

22.   Applicant's arguments with respect to claims 1-20 have been considered but are moot in

view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following documents have been made record of to further show the state of the art as it

pertains to path selection.

  Noel et al. U.S. Patent Number: 6,381,682

  O'Brien et al. U.S. Patent Number: 5,278,973

  Shigetomi et al. U.S. Patent Number: 6,496,883

  Rangachar U.S. Patent Number: 6,249,519

  Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The

examiner can normally be reached on M-F 9:00 A.M. to 5:00 P.M.

  If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746 7239 for regular

communications and (703) 746 7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305 3900.

NP
May 30, 2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100